DEVELOPMENT OF ALGORITHMS AND PROGRAMS FOR PROCESSING SPEECH SIGNALS ON VISUAL DSP ++ PLATFORM

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Abstract: Nowadays, digital signal processors or DSP (Digital Signal Processor) are very popular in the world and are even recognized as a separate field of science and technology.
Analog Devices A practical guide to self-study and practical application of one of the digital signal processors. It contains a detailed description of the processor, schemes of its practical use and programming technology. At present, the growth of innovation activity, despite the importance of innovation in the field of management for the socio-economic development of society, is growing mainly due to technological innovation. The problems of effective introduction and dissemination of innovative management technologies in the field of information and communication have not yet been sufficiently studied. Little attention is paid to the study of world experience in the use of innovative technologies in the management of information and communication and the possibility of adapting it to the conditions of Uzbekistan. Insufficient theoretical and methodological development of this problem has determined the relevance of the chosen topic and the main directions of dissertation research.

Keywords: algorithm, novices, programming, software visualization, signals, visual DSP++ platform.

Introduction

In the report of the President of the Republic of Uzbekistan Shavkat Mirziyoyev at the enlarged meeting of the Cabinet of Ministers on the main results of socio-economic development of the country in 2016 and the most important priorities of the economic program for 2017, ensuring the competitiveness of technologies created in our country. He stressed the need to pay serious attention to such issues as the creation of "know-how", the introduction of modern information and communication technologies, ie the implementation of systemic measures to ensure the production of high quality products and technological processes [1-9] and large enterprises, organizations and companies with a serious need to improve management systems. He also

noted that the associations do not take the necessary initiative in the introduction of information and communication technologies.
The success of the ongoing reforms in the country necessitates a radical change in the attitude of the public to information. In social work, information is becoming an auxiliary and secondary factor, a major factor influencing the organization of services, the economy, defense and politics. In this regard, the problems of rational formation and use of local government of information are of great importance in the development of the socio-economic sphere [10-17].
“Formation of local government of informatization in all spheres of economy and public life. The Decree of the President of the Republic of Uzbekistan No. PK-1730 of March 21, 2012 "On the development of computerization in the country and the introduction of information and communication technologies" also highlights the urgency of the issue.

The formation of a market mechanism in the economy requires the creation of the necessary conditions for the activities of the main market participants, producers and consumers, requires entrepreneurs to have an information environment in accordance with these mechanisms. This environment should provide information support to market participants at all stages of products, services and consumption, as well as in all areas of their activities. At the same time, an important task in the formation of the information infrastructure of the Republic of Uzbekistan is to create the best conditions for entrepreneurs to receive information.uaratishdir. This information is called "Business Information" or "Business Information" in the world.
The complexity of the problem is determined by the fact that it is characterized by the diversity of large-scale relations and must be solved in the context of changing the economic mechanism and its composition. Another important aspect of the issue is that today the relations between the state and economic entities are changing radically. The state's ability to fully influence the information market is insufficient. Finally, a number of shortcomings in the information and communication infrastructure of the Republic of Uzbekistan make it difficult to obtain information for the participation of the market and social relations. In this case, the solution of the problem requires non-standard solutions. A complete solution to this problem requires harmonization with the global dynamics of global information..Its peculiarity is that with the help of telecommunications and technology management, different countries and regions are rapidly integrating into a single performance management. Currently, the total volume of automated information resources in Uzbekistan is insufficient. In the recent past, they have been able to use only a small part of the resources, which are primarily planned for technical development, as a business media that meets market requirements. One of the problems in local government is the lack of adequate local and territorial governance in the public administration, which is aimed at a narrow range of consumers [18-20].
"Information technology is an entrepreneurial activity for the sale of goods, performance of works and provision of services, carried out with the use of information management.".
In other words, information technology is any agreement that takes place through a computer network in the use or exchange of ownership of information goods and services. Information technology uses not only Internet-based controls, but also "Information Stores" operating through BBS, VAN and other similar telecommunications networks.
Relevance:
With the development of modern information technology and the corresponding increase in data, the issue of data management is on the agenda.
When analyzing the software tools created in the field of application of information technology in the education system, we see that the presentation of information in the form of images is considered in a number of studies [21]. At the same time, many authors who create curricula on the computer are creating their own methods of presenting educational and scientific materials in the form of images, independently of each other.
Goals and objectives:
This master's dissertation consists of the creation of new automated control model methods, algorithms and tools using existing methods and information technology.
Practical significance:
Using the proposed management model is to increase the efficiency of the existing knowledge base management systems [22].

Scientific novelty:The modern world cannot be imagined without reading and processing information. The amount of information a person receives is growing exponentially. And this data can be processed by different information systems. Currently, the most effective way to convert analog signals to digital signals is the Visual DSP platform. The Visual DSP platform processes several ways to convert any data, audio and other analog signals into digital signals [23].

Object of research.Electronic document exchange system of the Higher Attestation Commission under the Cabinet of Ministers of the Republic of Uzbekistan.

Schematic of signal processors

This part of the paper provides an overview of the history of various signal processors and the technical characteristics of the ADSP-21XX signal processor family. In addition, it provides a practical diagram of the ADSP-2181 processor program, describes its architecture and program logic model, and describes the processor interrupt system [24].

Nowadays, digital signal processors or in short DSP (digital signal processor) have become very popular. This book removes the mystery of these components and allows students to independently develop and use them in their own designs.

Signal processors got their name from their internal ability to process audio and video signals. This is due to the high speed of these processors and the built-in special instruction system that supports digital filtering and fast Fourier conversion functions. The following are the main differences between signal processors and traditional microprocessors.

- Availability of hardware multiplier.
- availability of special data processing units.
- Special command system for digital signal processing.
- High performance.
- Built-in clock multiplier.
- RISC architecture.
- Ability to execute multiple commands at the same time.
- Harvard processor architecture.
- Ability to transmit commands and data via pipeline.
- Availability of round buffers.
- Advanced system of external interfaces.

Some types of this processor family also have a built-in analog-to-digital ADC converter and a DAC digital-to-analog converter, which provide direct analog signals to the processor, which are digitized. then processed digitally. the same processor. As a rule, the processing is a spectral analysis of the signal, ie. detect the presence of a certain amplitude frequency in this signal, filter the signal from unnecessary frequencies, compare the signal with the reference template signal, synthesize and create speech, compress and decompress audio and video signals, and so on. In the modern world, there are a large number of similar tasks in the most diverse areas of human activity. The solution to these problems is radio electronics, required in areas requiring radar, navigation, communications, medicine, automotive, aerospace and other sciences. Due to its importance, digital signal processing is now also recognized as a separate branch of science and technology. Apparently, a great future is opening up for these processors. Therefore, at the beginning of the development of signal processors, it is important to get acquainted with them in time so that in the future they do not seem difficult and inaccessible to us. According to him, a great future is opening up for these processors. Therefore, at the beginning of the development of signal processors, it is important to get acquainted with them in time so that in the future they do not seem difficult and inaccessible to us. According to him, a great future is opening up for these processors. Therefore, at the beginning of the development of signal processors, it is important to get acquainted with them in time so that in the future they do not seem difficult and inaccessible to us [25].

History of signal processors

Let’s take a brief tour of the development history of this processor family. The first signal processors appeared in the early 1980s. One of the first companies to start manufacturing these processors was Japan’s NEC Corporation, which produced the MPD7720 single-chip signal processor. However, this processor was not widely used because in 1982 it was replaced by a more efficient and advanced TMS32010 processor released

by Texas Instruments. Thanks to its successful architecture and a number of technical solutions, it has become practically the standard for signal processors. Below are the main specifications of this processor.

Data width 16 bits

Perform 5 million operations per second

RAM 256 words

The program memory capacity is 4K words

The amount of external memory connected is 4K words

The bit width of an arithmetic logic device is 32 bits

The multiplier is 6 × 16 bits and has a 32-bit result

I / O ports 16 bits

Number of I / O ports 8

The capacity of the external bus is 50 Mbit

The adoption of new micron technologies and the resulting increase in the degree of integration of chips allowed to significantly improve the characteristics of processors. And in the mid-1980s, second-generation signal processors emerged. These include the same Texas Instruments TMS320C25 and TMS320C5X processors. These processors are faster and have more memory. In addition, they have an improved interrupt management system and energy-saving modes of operation. Some processor models have reduced supply voltage. Shadow registers are created to automatically save work results when the program's hardware or software is interrupted.

In turn, Motorola has released the DSP56000 family of signal processors, which are 24-bit wide, have two internal X and Y data buses, are convenient for working with complex numbers, and have a high level of piping and parallelism. These features make these processors more efficient and convenient for processing digital signals.

Another manufacturer, AT&T Microelectronics, manufactures DSP16 series signal processors, which are characterized by cache memory and built-in high-speed, up to 30 MB parallel port.

Analog Devices Signal Processors entered the market with some technical parameters, as well as the ADSP-21XX series, which competes with the above models in terms of price. For example, the ADSP-21msp50 has built-in ADCs and DACs and costs several dollars at a time.

The development of signal processors did not stop, and in the late 1980s, third-generation processors from the above companies appeared on the market. A distinctive feature of this generation was the emergence of binary floating arithmetic, the increase in data bus width, memory, and application size. These processors include the TMS320C30 from Texas Instruments, the DSP96002 from Motorola, the DSP32C from AT&T Microelectronics, and the ADSP21020 from Analog Devices.

Later, signal processors from other companies appeared on the market. However, currently Texas Instruments, Motorola, AT&T Microelectronics and Analog Devices are the leaders in this field [26].

The history of the development of signal processors does not end there, and it can continue to tell, but the purpose of this book is not a historical event, but a practical guide to mastering and mastering the skills of working with these promising components.

Architecture of signal processors

This section describes the internal architecture of the ADSP-2181 signal processor of one of the analog devices and its connection examples.

Analog Devices have developed entire families of signal processors and are always continuing to market new models. Currently there are the following families: ADSP-21XX, Shark DSP, BlackFin DSP and others. However, despite the diversity of these groups, they all have a similar architecture. Families differ from each other, for example, in arithmetic units that support constant or floating point calculations. In addition, families differ in performance, data bus bit width, internal register structure, interfaces, and more. The differences between processors within a family are mainly in the size and organization of the internal memory and the type of interfaces installed. Each of the processors in this family has the following functional devices.

• ALU arithmetic logic unit.

• multiplier-accumulator.

• shearing device.

• Two generators of data addresses.
• Programming machine.
• Timer.
• serial multi-channel port.

Today we will talk about the architecture of one of the most common processors of the ADSP-21XX family, namely the processor ADSP-2181. This component is the most advanced in its family and includes the largest amount of memory and many built-in interfaces.

The ADSP-2181 signal processor is a single-chip chip available in 128-pin PQFP-128 or TQFP-128 packages. From the above information you can already get an overview of the capabilities of this processor. But for completeness, consider the block diagram shown in the figure diagram of the internal architecture of this chip. (Figure 1)

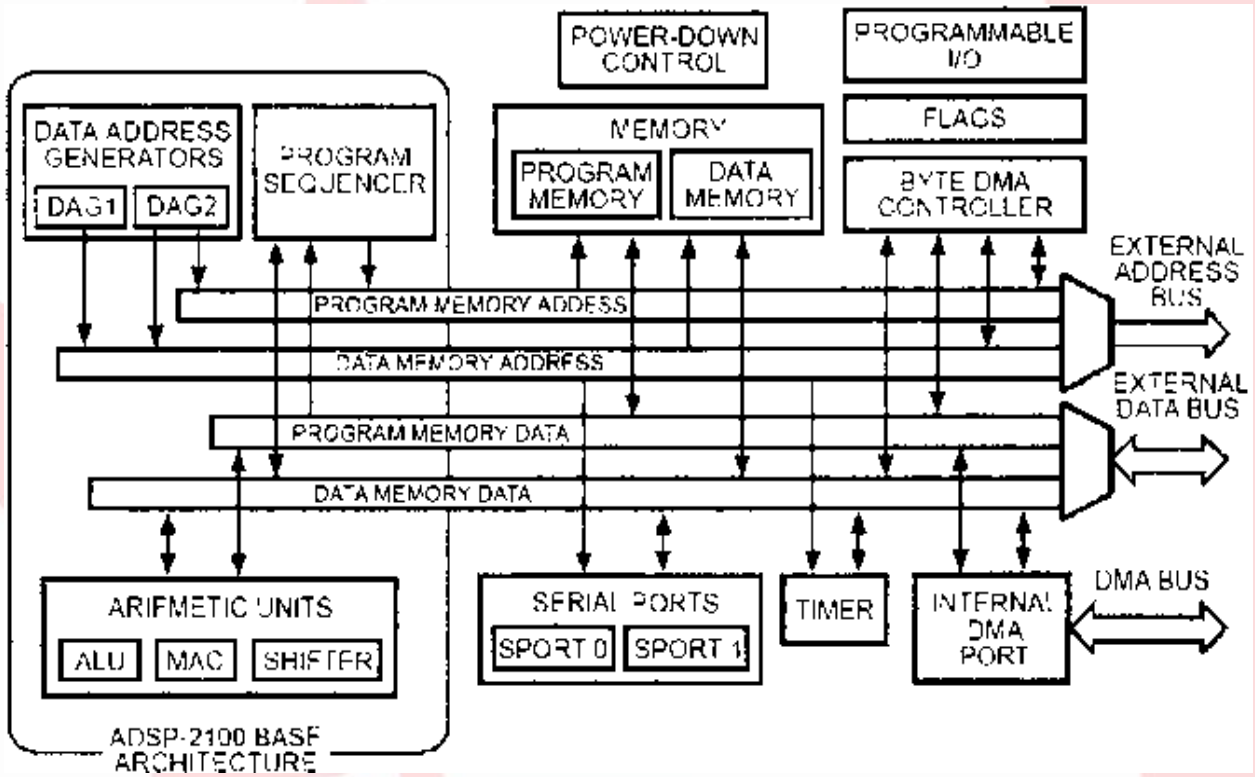


Figure 1. Block diagram of the chip's internal architecture

The processor internal address and data bus has a very advanced structure. These include the PROGRAM MEMORY ADDRESS bus, the DATA MEMORY ADDRESS data bus, the PROGRAM MEMORY DATA data bus, and the DATA MEMORY DATA data bus.

The diagram on the left shows the main architectural block of the entire ADSP-2100 BASE ARCHITECTURE family included in any processor in this family. It consists of the DATA ADDRESS GENERATORS data address generation block, the PROGRAM SEQUENCER program machine, and the ARITHMETIC UNITS arithmetic block.

The data address generator block has two generators - DAG1 and DAG2 - designed to reverse the address bits when the processor is performing fast Fourier Transform (FFT) operations.

The software machine supports operation with conditional jumps, subroutine calls, and return to the main program, thereby speeding up CPU performance in general.

The arithmetic unit includes the ALU arithmetic logic unit, the MAC battery multiplier, and the SHIFTER shift unit. The first of these blocks is designed to perform arithmetic and logic operations on data, and the second is designed to perform arithmetic multiplication of numbers. SHIFTER allows you to normalize numbers after performing arithmetic operations.

Look at the blocks at the top right of the diagram. The POWER DOWN CONTROL control unit controls the processor to switch to low power mode after executing the appropriate command, and to return from this mode after an interrupt or restart. The MEMORY unit consists of DATA MEMORY data memory and PROGRAM MEMORY memory. Thus, the RAM of the entire processor is divided into two independent parts according to the Harvard processor architecture. However, this instruction set of processors allows the program to be used to store data from memory. Programmable I / O PROGRAMMABLE I / O block, optional allows you to program multiple pins to input or output ra bit signals, which allows flexible use of these pins. The FLAGS flag block controls a three-bit pin organized as a signal output. Finally, the BYTE DMA CONTROLLER byte control block, abbreviated and hereinafter referred to as BDMA, provides fast hardware input and output via the processor's external data bus [27].

Now let's look at the blocks at the bottom right of the diagram. One of the most popular and useful is the SERIAL PORTS, which includes SPORT1 and SPORT2 serial ports. The unique feature of these ports is that they are programmable, synchronous and multi-channel. That's it. each of these ports is capable of receiving and transmitting data from a one-word to thirty-two-word serial bit stream. The length of each word in the stream can be from three to sixteen bits. This data transmission format is often used in the construction of telecommunication systems. Up to 32 codecs can be connected to such a port at the same time and 32 analog input-output channels can be received at their output. I agree - this is a powerful tool that can be applied in plab areas. In addition, the ports can be programmed for external or internal synchronization. The control pins of the ports can also be programmed for input or output.

The next block of the timer is the TIMER, which calculates the required time intervals and timer interruptions. An interrupt occurs when the timer counter is cleared, after which a value is loaded from the sixteen-bit register that stores the timer cycle.

Finally, the INTERNAL DMA PORT IDMA block of the internal port, abbreviated as IDMA, is used to organize direct access to the data memory and processor program memory via a sixteen-bit external bus. 'designed. This port plays an important role in working with the processor, as it loads the program and data directly into the processor's memory before starting it, starts the processor, and reads the data into memory while it is running. and write, as well as the performance of the processor [28].

The processor communicates with the outside world via fourteen-bit EXTERNAL ADDRESS BUS, twenty-four bit EXTERNAL DATA BUS, and sixteen-bit IDMA DMA BUS.

System outages

This chapter describes a system of interruptions that allows the processor to respond quickly to various events. The Interrupt Manager allows the processor to respond to eleven possible interruptions and restarts. Interruptions in the processor have a different priority, from 0 to 11. If any interruption occurs, the processor jumps to the subroutine to process the corresponding interrupt, the address of which is set to the vector of that interrupt. Interrupt vector addresses are located at the very beginning of the processor's program memory by means of four 24-bit command words, which allow a simple interrupt to be processed or exited in its place without having to go to the interrupt processing programmer. Otherwise, you can unconditionally switch to the interrupt processing order with the pass command.

The ADSP-2181 has four pins to support external suspension: IRQ2, IRQL0, IRQL1, and IRQE. In addition, SPORT1 can be reconfigured to FLAG_IN, FLAG_OUT flag pins, and the processor can have two more external interrupt inputs instead of internal SPORT1 interrupts due to IRQ0, IRQ1 interrupts. As a result, the processor can have a total of six external interrupts.

In addition to external interrupts, the processor also has internal interrupt sources. Sources of internal interruptions are a timer, a BDMA byte port, two SPORT1 and SPORT2 serial ports, a software reset stop, and low voltage interruptions.

All interruptions, except for the mask and reset, can be turned off using the IMASK register. You can also programmatically create or delete some interruptions using the IFC registry [29].

The processor affects the signal level at the IRQL0 and IRQL1 interrupt pins. The IRQE interrupt occurs at the edge of the signal change at this pin. The sensitivity of the processor to IRQ0, IRQ1 and IRQ2 signals is determined using software using the ICNTL register.

Modern models of signal processors used in audio signals

Signal processors appeared in the early 80s. The first well-known signal processor TMS32010 was manufactured in 1982 by Texas Instruments, with a capacity of several MIPS (million instructions per second), based on 1.2mkm technology. Following in the footsteps of Texas Instruments, other firms began producing RSP. Texas Instruments is currently the leader in RSP production, accounting for nearly half of the controller market. In second place in terms of production is the RSP of Lucent Technologies, which accounts for a third of the devices. In addition, the RSPs of Analog Devices and Motorola are the leaders, accounting for about a quarter of the market for approximately equal RSPs. Of the remaining manufacturing firms, Samsung, Zilog, Atmel and others will remain in the remaining 5-6% of the RSP market. Texas Instruments, a leading manufacturer in the industry, is an RSP fashion installation firm. The policies of leading companies in production and development shifts are different. Currently, the RSP capacity reaches 8800 MIPS and they are produced on the basis of 0.65 μm-0.1 μm technology. The clock frequency reaches 1.1 GHz. Produced on the basis of 65 μm-0.1 μm technology. The clock frequency reaches 1.1 GHz. Produced on the basis of 65 μm-0.1 μm technology. The clock frequency reaches 1.1 GHz.

The policy orientation of Lucent Technologies is focused on large firms that produce the final equipment, and they offer their products through a distribution network, while not employing large advertising companies. The firm has specialized in RSPs for telecommunications equipment, currently focusing on promising areas such as the creation of commercial communication stations.

Analog Devices has an active marketing policy towards the above-mentioned firm, for example, the abbreviations of this firm's RSPs SHARK and Tiger SHARK. In the technical field, the company's RSPs are aimed at optimizing energy consumption and building multi-processor systems [30].

Motorola is deploying its own processors, making extensive use of its distribution network, which is divided into private networks. Motorola was one of the first in the RSP architecture to create a signal processor and a microcontroller within a single crystal at the same time, that is, to create a unique system that simplifies the schematic solution and makes it easier to work with device creators.

Examples of common models of signal processors:

Motorola 56002,96002,

Intel i960,

Analog Devices 21xx, 210xx,

Texas Instruments TMS320Cxx.

Figure 2.1. Company logos of major RSP manufacturers

Texas Instruments (TI) accounts for half of the digital signal processing processors market. The same firm developed the first digital signal processing processor in 1982. The TMS32010 digital signal processing processor was used in the Speak and Spell game, and was also used in the talking Julie doll. All signal processing processors from Texas Instruments are manufactured under the brand TMS3200xxx.

Russia also produces digital signal processing processors, but in reality they are cheaper than foreign manufacturers. For example, the Institute of Electronic Research currently produces digital processors for 16-bit 5 MIPS performance signals.

Table 1. Basics of DSP manufacturers and their market share

Company name	DSP market share
Texas Instruments	54.3%
Freescale Semiconductor	14.1%
Analog Devices	8.0%
Philips Semiconductors	7.5%
Agere Systems	7.3%
Toshiba	4.9%
DSP Group	2.2%
NEC Electronics	0.6%

Fujitsu	0.4%
Intersil	0.3%
The remaining companies	0.5%

The best modern RSPs can be compared on the following features:

Video processing, video surveillance, digital cameras, 3D graphics	TMS320DM64x / DaVinci, TMS320C64xx, TMS320C62xx (TI), PNX1300, PNX1500, PNX1700 (Philips), MPC52xx (Freescale)
Audio processing, speech recognition, sound synthesis	TMS320C62xx, TMS320C67xx (TI), SHARC (Analog Devices)
Portable media devices	TMS320C54xx, TMS320C55xx (TI), Blackfin (Analog Devices)
Wireless communication, telecommunications, modems, network devices	TMS320C64xx, TMS320C54xx, TMS320C55xx (TI), MPC7xxx, MPC86xx, MPC8xx PowerQUICC I, MPC82xx PowerQUICC II, MPC83xx PowerQUICC II Pro, MPC85X, PowerQUICC ()
Transmission control, power conversion, automotive electronics, home appliances, office equipment	TMS320C28xx, TMS320C24xx (TI), ADSP-21xx (Analog Devices), MPC55xx, MPC55xx (Freescale)
Medicine, biometrics, measuring systems	TMS320C62xx, TMS320C67xx, TMS320C55xx, TMS320C28xx (TI), TigerSHARC, SHARC (Analog Devices)

Clock frequency - 1 GHz and higher;
Multi-core;
Availability of two-level cache;
Installation of multi-channel controllers with direct access to memory;
Multiple MIPS i MFLOPS fast performance level;
Execution of up to 8 parallel instructions per clock;
Compatible with standard tires.
Modern signal processors provide tremendous performance, which is due to technological and architectural advances. All RSPs provide the same speed, and there are many types of signal processors, each of which is designed to solve a specific problem, and can cost in the range of US $ 1.50 - $ 180.
TMS320C6457 fixed comma RSP:
The clock frequency is 850-MHz, 1-GHz, and 1.2-GHz
Productivity 8000 and 9600 MIPS / MMACS (at 16-bit)
L1P Program - 32K-Byte
L1D Data - 32K-Byte
L2 - 2Mb
L3 ROM - 64 K-Byte
Ethernet MAC - 10/100/1000 Mb /
Total addressable memory 32 Mb

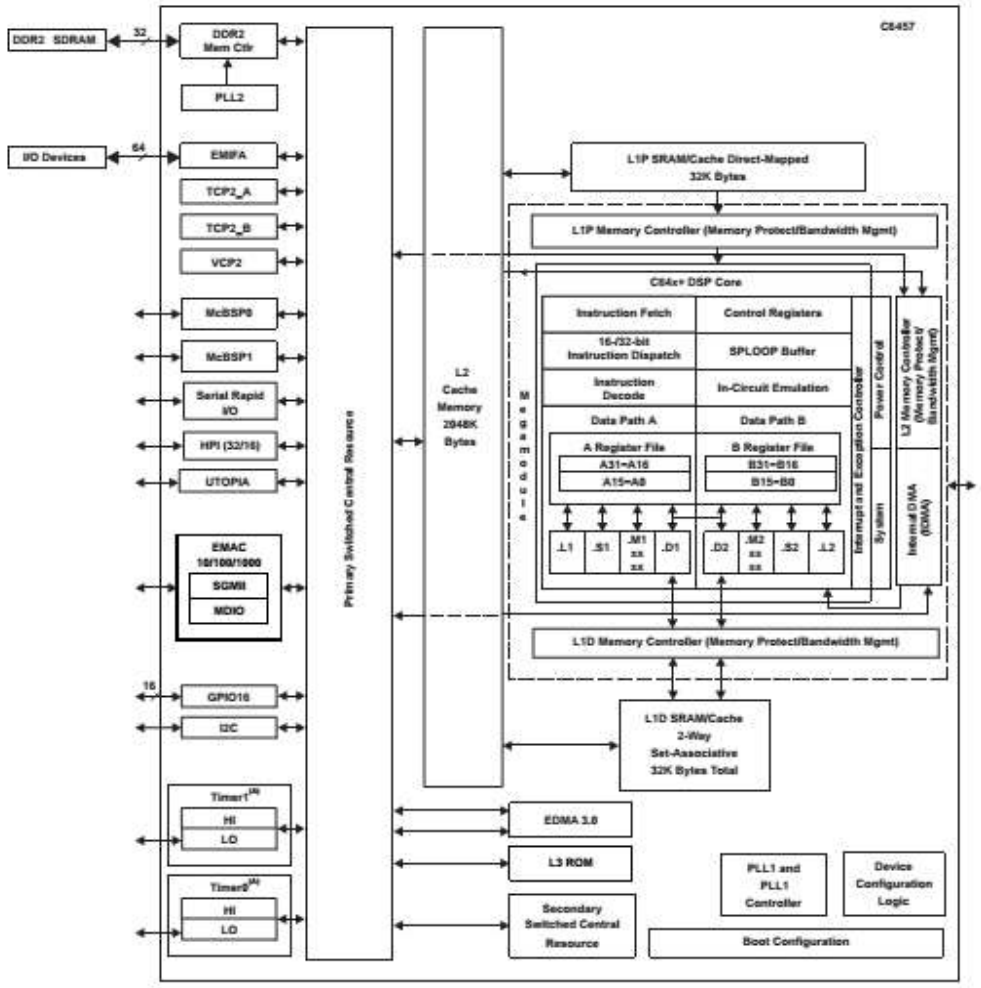


Figure 2.2. TMS320C6457 Structural drawing of RSP

Modern models of signal processors are also used in smartphones, for example the Snapdragon 600 processor. It has a Hexagon QDSP6 digital signal processor that performs simple tasks, such as putting on music, providing phone conversations, and the like.

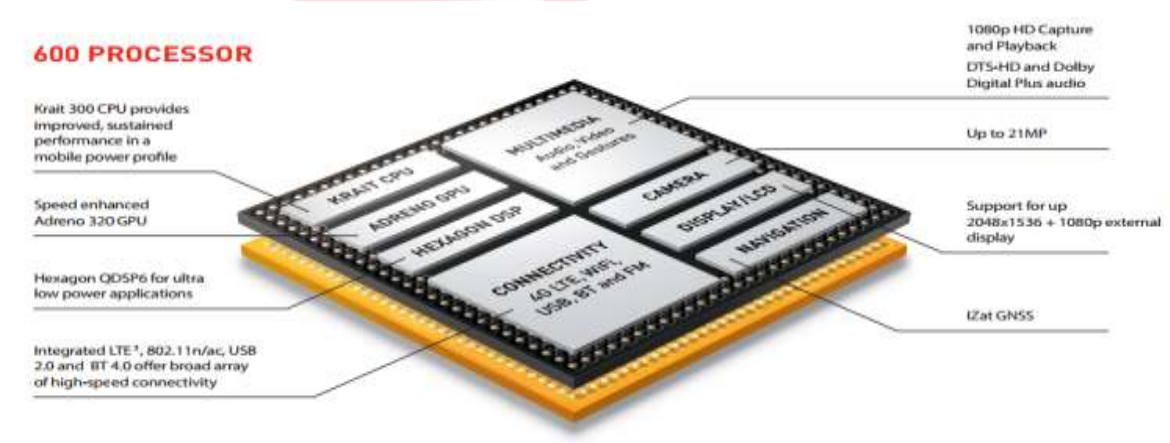


Figure 2.3. Snapdragon 600 processors

2.2. Architecture of multi-core signal processors

As a result of the development of data filtering methods, the algorithms that process them also change. The consumer, on the other hand, needs to increase its quality during image and sound playback, which places additional demands on digital processing devices for these signals. Multi-core signal processors can help solve these problems. In such processors, several cores provide processing for dynamically variable requirements.

Basic architectures of multi-core processors:

VLIW - Architectural signals are very long commands based on digital processing processors. The main difference between VLIW-processors is that during the compilation stage, the command codes are grouped into large "super commands" and executed in parallel.

SIMD - allows a single command to be executed on different data used in parallel with the processor, thus increasing the relative efficiency of some algorithms. For example, the SIMD multiplication command can perform 2 or 3 multiplications on different unwanted operands in one clock in parallel. But there are some complexities in terms of programming. For example, ensure that 1 in 4 data arrives.

Superscalar (Superscalar) - processors are a set of parallel operating commands that have the ability to execute several commands at the same time, that is, they use the parallelization of the flow of commands. Supercalar processors plan to execute commands based on information about the operation of the operating blocks and the relationship between the data.

VLIW.Typically, such processors use the RISC-architecture, in which each operation is performed in a separate operating module. Features of such processors include:

A large set of operating modules that work independently of each other. Such a set of modules includes:

Arithmetic:

Module of arithmetic operations and comparison operations;

Logical Operations Module;

and a floating-point number multiplication module;

Variable generation module.

Address generation module, including linear and cyclic buffers;

The need for an optimized compiler for each processor model, as changes in the composition and functions of the computing blocks between the models, leading to a change in the set of instructions that can be executed simultaneously

Necessity in the presence of very wide data bus (128 bits), because the code of operations consisting of independent commands (up to 8) must be obtained from a single reference

Requirements for program memory size are associated with large lengths of operations

Typically, if the processor consists of several identical modules, the assembler has the ability to specify only the type of operating module when creating a program, and the exact device is determined by the compiler. On the one hand, it simplifies the programming of such devices, on the other hand, it allows them to use their resources efficiently.

VLIW-architectural signals are based on very long commands of digital processing processors, which allow independent operating modules to execute commands consisting of simple short commands simultaneously, while each command rates a single operation (RISC-processor operating principle). Examples of digital processing processors for such architectural signals are TMS320C62XX, TMS320C64XX, TMS320C67XX, each with 8 operating modules, two 32 32-bit registry files, and divided into two groups. The performance of digital processing processors for TMS320C6416 signals is 4800 MIPS, 2000 MIPS for TMS320C6202 and 1000 MFLOPS for TMS320C6416.

Motorola's MSC810X digital signal processing processors have a capacity of 1,200 MIPS and have 4 AMQs in the crystal and a filter coprocessor.

SIMD.The growth of multimedia applications for personal computer systems Many general-purpose processor manufacturers have incorporated multimedia extensions into their command set architecture. As a rule, these extensions take special forms, single-command, multi-data (SIMD), which perform the same parallel operations on a specific number of operands. Operands are typically all 8-bit, 16-bit, or 32-bit, placed in 32-bit or 64-bit registers. This is why these commands of the SIMD are called embedded arithmetic commands. SIMD is not an architecture class, but an architectural method that can be used in any architecture class. By allowing the SIMD to perform the same job on different data used in parallel with the processor, the zi increases the productivity of algorithms. For example, a SIMD multiplication command can perform two or three multiplications on different sets of operands entering in parallel on a single clock. This method can significantly increase the computational level for some vector operations that are more commonly used in

multimedia and signal processing applications. SIMD-enabled digital signal processors differ in the operating devices that support SIMD operations.

Analog Devices, for example, have replaced the basic standard architecture of the ADSP-2106x RSP with a floating comma, adding a second module set of performance that accurately replicates the initial set. The new architecture is called ADSP-2116x. Each set of execution modules in the ADSP-2116x includes MAC, ALU, and converter modules, and each has a set of individual operand registers. The enlarged architecture can issue a single command, and in some algorithms can effectively run it in parallel in both execution modules, effectively using different productivity of data ambiguity.

Nowadays, the SIMD architecture is a complex target for HLL compilers, and most commercial digital signal processors must be programmed in assembler language. Higher programming languages such as C cannot be used to show word parallelism, which makes it difficult for compilers to obtain such parallelism.

Superscalar.Supercalar processors are a set of parallel operating commands that have the ability to execute several commands at the same time, i.e. they use the parallelization of the command stream. But compared to VLIW, they have two features:

Processor commands are not grouped into blocks, each of which falls independently of the processor.

Parallel commands are grouped within the processor based on the content and the connection between the operating block and the data.

Using the given approach, the following shortcomings of VLIW can be avoided:

Inefficient use of a large group of operations in memory;

The relationship between the compiled code and the content of the operating modules of a given processor.

This leads to a significant complication of the processor circuit in solving problems and the emergence of a command execution scheduling module.

Supercalar processors plan to execute commands based on information about the operation of the operating blocks and the relationship between the data. For example, the arithmetic operation response cannot be executed before the save command computation operation, even if the memory access module is currently empty. This feature does not allow a single set of commands to be executed differently at different times of the program and to determine the exact value of performance. This is especially important for real-time systems, as the worst result is that the processor resources are not fully utilized.

Thus, evaluating the performance of digital processing processors to superscalar signals in such systems remains an open problem. Digital processing processors for VLIW-architecture parallel superscalar signals have high performance. These include the TIGERSHARC processor, ADSP-TS001 (300 MFLOPS) and ADSP-TS201S (1200 MMASS for 32-bit data and 4800 MMASS for 16-bit data).

But as parallelism increases, so does the number of registers and functional blocks that provide them, as well as the cost and complexity of control blocks. Given the strict requirements placed on the system of installed RSPs, superscalar architecture cannot be said to be the most cost-effective architectural choice.

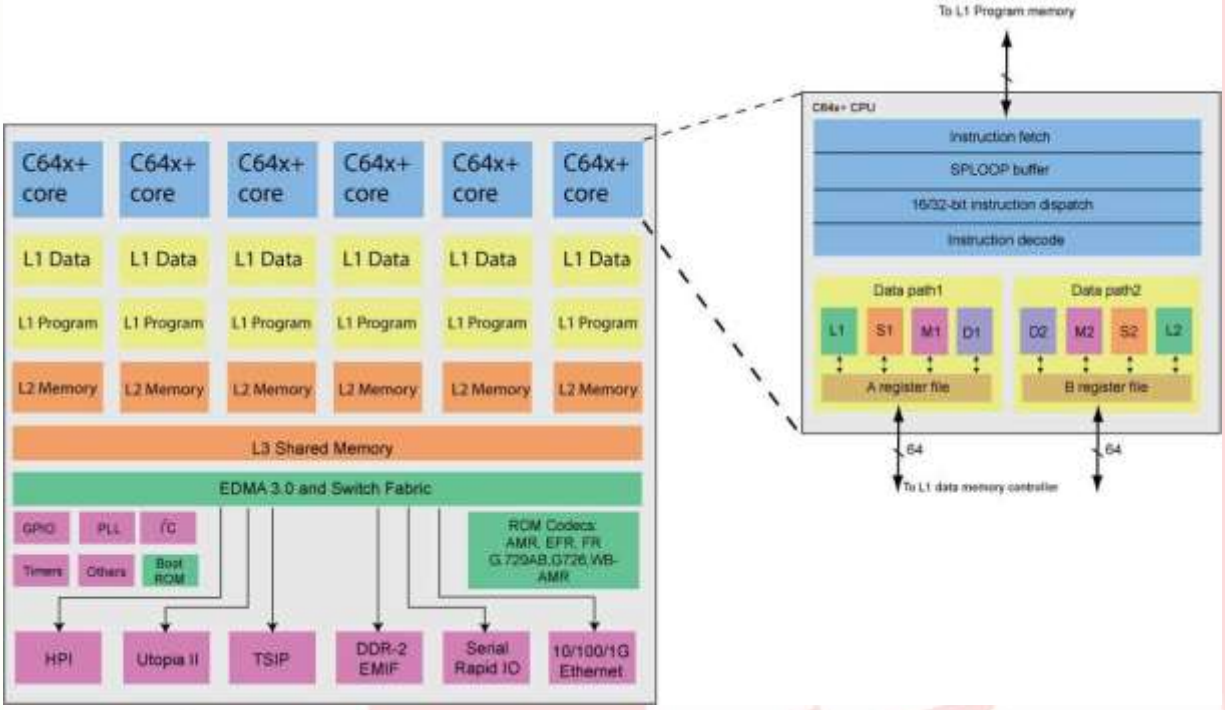
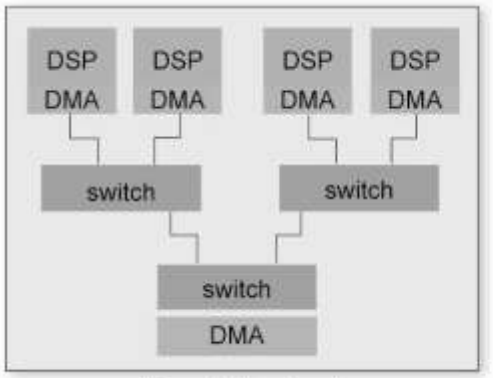
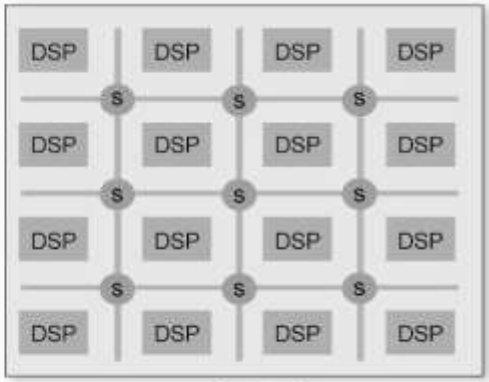


Figure 2.4 Typical structure of multi-core signal processor platforms (on the example of Texas Instruments TNETV3020 multi-core signal processor)



hierarchal network



mesh netwok

2.5. Interconnection types of multi-core signal processor architecture

Multi-core digital signal processors also have homogeneous and heterogeneous core architectures:

Homogeneous architecture -all the cores of the processor are the same and the performance functions are the same, for example, Intel Core Duo, Sun SPARC T3, AMD Opteron.

Heterogeneous architecture- Processor cores perform different functions. As an example: IBM, Sony and Toshiba are Cell processors under the company mergers, one core of which is a general-purpose PowerPC, and the rest are specialized processors.

Table 3. Multi-core signal processor platforms

	TI	Freescale	picoChip	Tilera	Sandbridge
Processor	TNETV3020	MSC8156	PC205	TILE64	SB3500
Architecture	Homogeneous	Homogeneous	Heterogeneous	Homogeneous	Heterogeneous
The amount of nuclei	6 DSPs	6 DSPs	248 DSPs 1 GPP	64 DSPs	3 DSPs 1 GPP
Topology	Hierarchical	Hierarchical	-	-	Hierarchical
Application	Wireless Video VoIP	Radio	Radio	Video Wireless networks	Radio

Modern multi-core digital signal processors can be identified by the type of core in the chip and include a homogeneous or heterogeneous architecture [31].

2.3. Command system and addressing in multi-core signal processors

Command system is a part of computer architecture related to programming, data type, commands, registers, addressing modes, memory architecture, interruptions and external input / output.

Types of commands:

Data processing and memory operations

Arithmetic - logical operations

Flow control operations

Advanced operations:

Move large memory blocks;

Calculation on floating-point numbers (sine, cosine);

Commands that use AMQ and memory, not AMQ and registry.

Figure 2.6. Types of command systems

Digital signal processors are mainly limited RISC command computing devices. Conveyor processing mode is used in digital signal processors. However, several different commands are executed at the same time.

As an example, Motorola's DSP56300 CPU architecture can be thought of as consisting of 3 functional blocks running in parallel: an arithmetic logic device (ALU), an address-forming block (AGU), and an application control block. The goal of the command system is to ensure that each of these modules is kept busy during each command cycle, while achieving maximum speed and minimum program size.

The command set is divided into several groups:

Arithmetic;

Logical;

Bit Manipulation;

Cycle (Loop);

Move;

Program Control.

Arithmetic commands perform all arithmetic operations on arithmetic logic device data.

Logical commands execute all logical commands in the arithmetic logic device data in a single loop of the command (except ANDI and ORI). Bit control commands check the status of any bit in the memory cell and then additionally correct, clear, or invert the bit. The hardware DO cycle is performed without the additional cost of cycles, i.e. it works like a straight line code. Replacing a straight-line kd with DO cycles can significantly reduce program memory. Move commands allow data to be moved.

Program management commands include transitions, conditional transitions, and other commands that affect the application cache and so on.

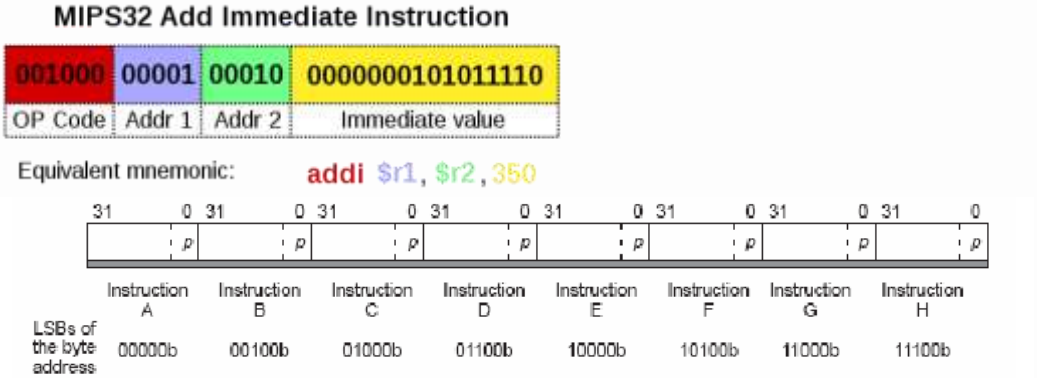


Figure 2.7. Example of command structures

The following information is included in the description of each command:

Name and mnemonics: Mnemonics are marked in bold for ease of reference.
Assembler Syntax and Operation: The appropriate operation for each syntax of the command is described symbolically. If there are several operations on a single line in the operation area, these operations are not necessarily performed in order, but are assumed to be performed in parallel as a rule.
Description: A complete description of the command text is provided so that the user can know the command in situations that may occur while using this command.
Code states: Status registers are represented by status code bits that can be affected by the command. Not all bits in the status register are used either.
Command format: command field, operation code command, as well as word extension commands are defined for each command syntax.
Most digital signal processors require the calculation of the sum of the series of serial multiplications. To perform this type of operation, a special multiplier and (in the next step) assembly block subdivision is required.
The MAC consists of a special register called a multiplier and a battery. MACs are of the following types
MAS(S = A * B + C)
used to perform functions.
MAS performs fast single-cycle operations: multiplication, addition multiplication. In MAS, operations are performed on numbers expressed in binary sequence form. Although multiplication and addition are two different types of operations, they can be performed in parallel. When the multiplier calculates its operands, the accumulator collects the previous multiplications. During the first multiplication, the battery is empty, that is, it waits for the task, and at the last multiplication, the multiplier is idle. Thus, the NQ1 loop is required to calculate the number of N operands.

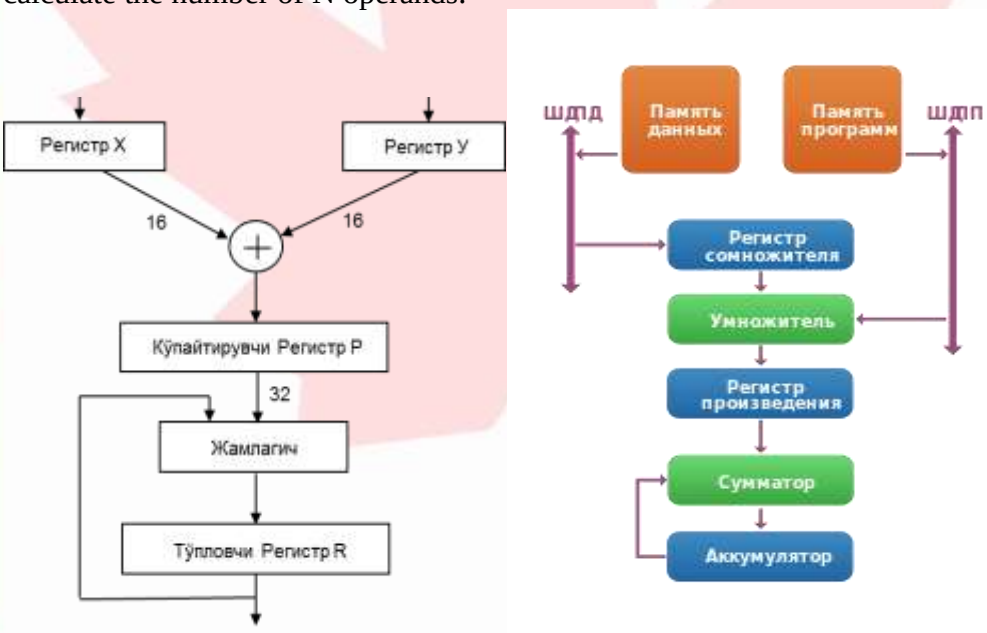


Figure 2.8. MAS structure
In the case shown in the figure, one of the operands is stored in the program memory, one in the data memory, so here the command is executed in 1 clock and the total execution time of the loop is equal to n clock. It should be noted here that in order for MAS 1 to actually run, and at the same time the command does not re-select its code (which requires an additional clock), the MAS must be executed within a special command of the cycle. The following methods should be used to prevent overflow and loss of value:
Use of switches at the MAC inputs and outputs;
Ensuring that bits are stored in the battery;
Using the saturation (saturation) logic.
Conductors can be provided to normalize the data at the MAC input and to restore the same data at the output [32].

Security bits

Since the normalization process does not give a clear result, it is not advisable to use it for some applications. In such cases, there is another alternative way by providing additional bits, called bits stored (protected) in the battery, so that the overflow error does not occur. Here, the addition / subtraction block must be changed accordingly to control the additional bits of the battery. Overflow or loss of values occurs when the result exceeds the limits of the most positive number or the lowest negative number, the battery does this. can do. And so, overflow or loss of value errors can be solved by loading the battery with a positive number that can operate when the battery is full and a negative number limit in the event of a value loss. This is called saturation (saturation) logic.

When the condition of overflow or loss of value in the saturation (saturation) logic is met, the battery is charged with a positive or negative number calculated by (by) the MAS device.

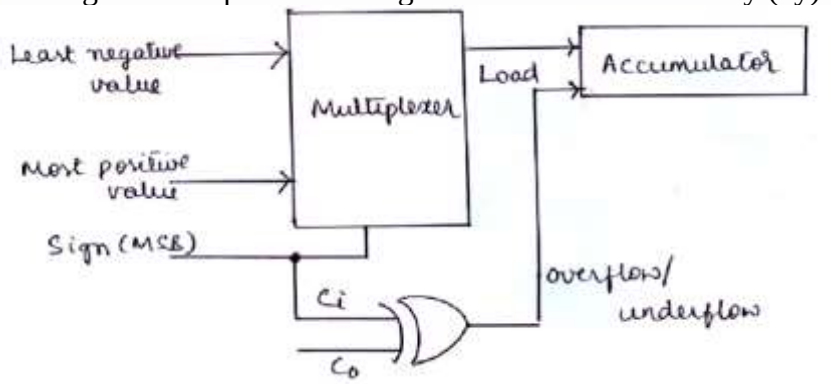


Figure 2.9. Schematic view of saturation (saturation) logic

When operations are performed on floating-point numbers, single rounding and double rounding (typical for RSPs) can be performed [33]. One-time rounding is also called fused multiply-add (FMA) or fused multiply-accumulate (FMAC). This command (in the absence of hardware realization) allows you to more efficiently perform multiplication of vectors and matrices, division by square root, and calculation of polynomials (polynomials) according to the Gorner scheme. Using a fast FMA result collection can increase and speed up the accuracy of most calculations:

Scalar multiplication;

Multiplication of matrices;

Evaluation polynomial (e.g., Gorner, as mentioned above);

Newton's method for evaluating function.

References

1. Urinov, K. O., Jumanov, K. A., Khidirov, A. M., Urinov, S. K., Abdiyev, J. M., Jumaboyev, T. A., & Eshmirzayev, M. R. (2020, April). Magnetocaloric effect in polycrystalline cobalt. In Journal of Physics: Conference Series (Vol. 1515, No. 2, p. 022079). IOP Publishing.
2. Saidov, A. S., Saparov, D. V., Usmonov, S. N., Kutlimratov, A., Abdiev, J. M., Kalanov, M., ... & Akhmedov, A. M. (2021). Investigation of the Crystallographic Perfection and Photoluminescence Spectrum of the Epitaxial Films of (Si2) 1-x (GaP) x Solid Solution, Grown on Si and GaP Substrates with the Crystallographic Orientation (111). Advances in Condensed Matter Physics, 2021.
3. LEYDERMAN, A., Saidov, A. S., USMONOV, S., Abdiyev, J. M., & Suyarov, Q. T. (2021, February). INFLUENCE OF WEAK GRADED GAP ON INJECTION DIFFUSION REGIMES OF CURRENT TRANSPORT IN SEMICONDUCTOR PN-STRUCTURES. In Congress Dates (p. 40).
4. Raufovich, M. R., & Muzaffar o'g'li, A. J. (2022). THE ROLE OF TEACHER AND STUDENT COOPERATION IN THE MODERN EDUCATIONAL PROCESS OF GOOGLE DOCS. Web of Scientist: International Scientific Research Journal, 3(1), 579-589.
5. Abdiev, J., Safarov, O., & Julanov, H. (2022). Study of the properties of polymer composites–reinforcement based on glass and basalt fibers. Eurasian Scientific Herald, 7, 77-88.
6. Urinov, K. O., Jumanov, K. A., Khidirov, A. M., Urinov, S. K., Abdiyev, J. M., Jumaboyev, T. A., & Eshmirzayev, M. R. (2020). Magnetocaloric effect in polycrystalline cobalt. In Journal of Physics: Conference Series (Vol. 1515, p. 022079).

7. Urinov, K. O., Jumanov, K. A., Khidirov, A. M., Urinov, S. K., Abdiyev, J. M., Jumaboyev, T. A., & Eshmirzayev, M. R. (2020). Magnetocaloric effect in polycrystalline cobalt. In JOP Conference Series: Metrological Support of Innovative Technologies (pp. 22079-22079).
8. Urinov, K. O., Jumanov, K. A., Khidirov, A. M., Urinov, S. K., Abdiyev, J. M., Jumaboyev, T. A., & Eshmirzayev, M. R. (2020, April). Magnetocaloric effect in polycrystalline cobalt. In Journal of Physics: Conference Series (Vol. 1515, No. 2). IOP Publishing.
9. Urinov, K. O., Jumanov, K. A., Khidirov, A. M., Urinov, S. K., Abdiyev, J. M., Jumaboyev, T. A., & Eshmirzayev, M. R. (2020, April). Magnetocaloric effect in polycrystalline cobalt. In Journal of Physics Conference Series (Vol. 1515, No. 2, p. 022079).
10. Saidov, A. S., Saparov, D. V., Usmonov, S. N., Kutlimratov, A., Abdiev, J. M., Kalanov, M., ... & Akhmedov, A. M. (2021). Investigation of the Crystallographic Perfection and Photoluminescence Spectrum of the Epitaxial Films of (Si2) 1-x (GaP) x Solid Solution, Grown on Si and GaP Substrates with the Crystallographic Orientation (111). Advances in Condensed Matter Physics, 2021.
11. Bolkievna, I. A. LEARNING FROM UZBEK AND PERSIAN TRADITIONS: THE ROLE OF ENVIRONMENTAL PERCEPTIONS IN THE CREATION OF SPACE IS A GARDEN-CREATING PARADISE.
12. Saidov, A. S., Saparov, D. V., Usmonov, S., Kutlimratov, A., Abdiev, J. M., Kalanov, M., ... & Akhmedov, A. M. (2021). Investigation of the Crystallographic Perfection and Photoluminescence Spectrum of the Epitaxial Films of (Si 2) 1-x (GaP) x 0≤ x≤ 1 Solid Solution, Grown on Si and GaP Substrates with the Crystallographic Orientation (111). Advances in Condensed Matter Physics, 2021.
13. Saidov, A. S., Saparov, D. V., Usmonov, S. N., Kutlimratov, A., Abdiev, J. M., Kalanov, M., ... & Akhmedov, A. M. (2021). Investigation of the Crystallographic Perfection and Photoluminescence Spectrum of the Epitaxial Films of (Si2)(GaP) x (0≤ x≤ 1) Solid Solution, Grown on Si and GaP Substrates with the Crystallographic Orientation (111).
14. Saidov, A. S., Saparov, D. V., Usmonov, S. N., Kutlimratov, A., Abdiev, J. M., Kalanov, M., & Razzakov, A. S. (2021). Investigation of the Crystallographic Perfection and Photoluminescence Spectrum of the Epitaxial Films of (Si [sub. 2])[sub. 1-x](GaP)[sub. x](0≤ x≤ 1) Solid Solution, Grown on Si and GaP Substrates with the Crystallographic Orientation (111). Advances in Condensed Matter Physics, 2021.
15. Saidov, A. S., Saparov, D. V., Usmonov, S. N., Kutlimratov, A., Abdiev, J. M., Kalanov, M., ... & Akhmedov, A. M. (2021). Investigation of the Crystallographic Perfection and Photoluminescence Spectrum of the Epitaxial Films of (Si 2) 1-x (GaP) x 0≤ x≤ 1 Solid Solution, Grown on Si and GaP Substrates with the Crystallographic Orientation (111). Advances in Condensed Matter Physics.
16. LEYDERMAN, A. Y., SAIDOV, A., USMONOV, S. N., ABDIYEV, J., & SUYAROV, Q. (2021, February). INFLUENCE OF WEAK GRADED GAP ON INJECTION DIFFUSION REGIMES OF CURRENT TRANSPORT IN SEMICONDUCTOR PN-STRUCTURES. In Congress Dates (p. 40).
17. LEYDERMAN, A. Y., SAIDOV, A., USMONOV, S. N., ABDIYEV, J., & SUYAROV, Q. (2021, February). INFLUENCE OF WEAK GRADED GAP ON INJECTION DIFFUSION REGIMES OF CURRENT TRANSPORT IN SEMICONDUCTOR PN-STRUCTURES. In Congress Dates (p. 40).
18. Leiderman, A. Y., Saidov, A. S., & Abdiyev, J. M. (2021). INJECTION DIFFUSION PROCESSES IN THE WEAK LINEAR GRADED-BAND SEMICONDUCTOR pn-STRUCTURES. Euroasian Journal of Semiconductors Science and Engineering, 3(1), 3.
19. Leiderman, A. Y., Saidov, A. S., & Abdiyev, J. M. INJECTION DIFFUSION PROCESSES IN THE WEAK LINEAR GRADED-BAND SEMICONDUCTOR pn-STRUCTURES. Journal of Semiconductors, 3(1), 3.
20. Abdiev, J., Safarov, O., & Julanov, H. (2022). Study of the properties of polymer composites–reinforcement based on glass and basalt fibers. Eurasian Scientific Herald, 7, 77-88.
21. Abdiev, J., Safarov, O., & Julanov, H. Study of the properties of polymer composites–reinforcement based on glass and basalt fibers.
22. Abdiev, J., & Safarov, O. (2022). BASALT FIBER-BASIC (PRIMARY) CONCEPTS. Web of Scientist: International Scientific Research Journal, 3(4), 212-240.
23. Abdiev, J., & Safarov, O. BASALT FIBER-BASIC (PRIMARY) CONCEPTS.

24. KUŞÇULU, N. (2021). Congress Dates.
25. Abdiev, J., Safarov, O., & Julanov, H. (2022). Study of the properties of polymer composites–reinforcement based on glass and basalt fibers. Eurasian Scientific Herald, 7, 77-88.
26. Abdiev, J., Safarov, O., & Julanov, H. (2022). Study of the properties of polymer composites–reinforcement based on glass and basalt fibers. Eurasian Scientific Herald, 7, 77-88.
27. Abdiev, J., Safarov, O., & Julanov, H. Study of the properties of polymer composites–reinforcement based on glass and basalt fibers.
28. Bolkievna, I. A., & AbdievMuzaffar o'g'li, J. (2022). LEARNING FROM UZBEK AND PERSIAN TRADITIONS: THE ROLE OF ENVIRONMENTAL PERCEPTIONS IN THE CREATION OF SPACE IS A GARDEN-CREATING PARADISE. Web of Scientist: International Scientific Research Journal, 3(4), 188-211.
29. Bolkievna, I. A. LEARNING FROM UZBEK AND PERSIAN TRADITIONS: THE ROLE OF ENVIRONMENTAL PERCEPTIONS IN THE CREATION OF SPACE IS A GARDEN-CREATING PARADISE.
30. KUŞÇULU, N. (2021). Congress Dates.
31. Abdiev, J., & Safarov, O. BASALT FIBER-BASIC (PRIMARY) CONCEPTS.
32. KUŞÇULU, N. (2021). Congress Dates.
33. KUŞÇULU, A. P. D. N. Access Date: 22.06. 2021.